Overview of the LISA Phasemeter

Daniel Shaddock, Brent Ware, Peter Halverson, Robert Spero and Bill Klipstein

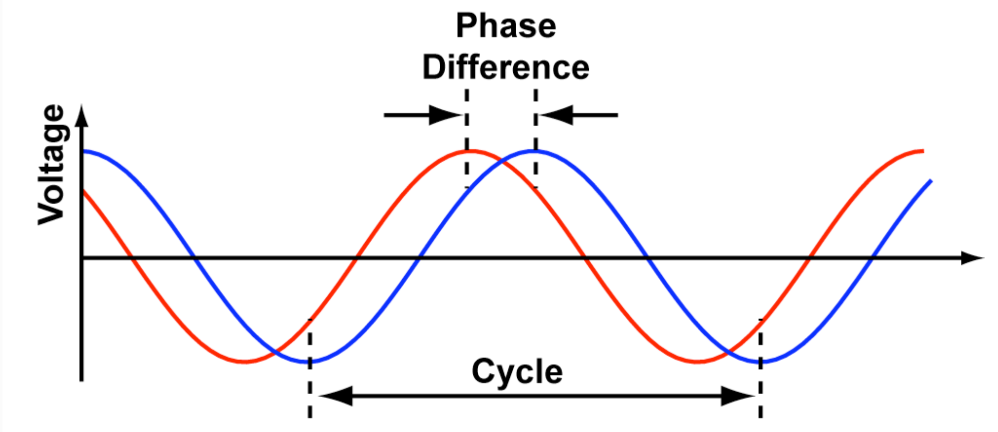
Jet Propulsion Laboratory,

California Institute of Technology

GSFC-JPL

Phasemeter

- The output of the photoreceivers will be a *beat note* (a sine wave).
- Gravitational wave information is contained in the phase of this beat note.
- A ***phasemeter*** measures the relative phase of two electronic signals.



1 cycle of phase shift = 1 wavelength distance change

Phasemeter

Science Measurement
High accuracy measurement for extracting gravitational wave signals.

Laser Locking Output
Low latency output for laser phase-locking/arm-locking

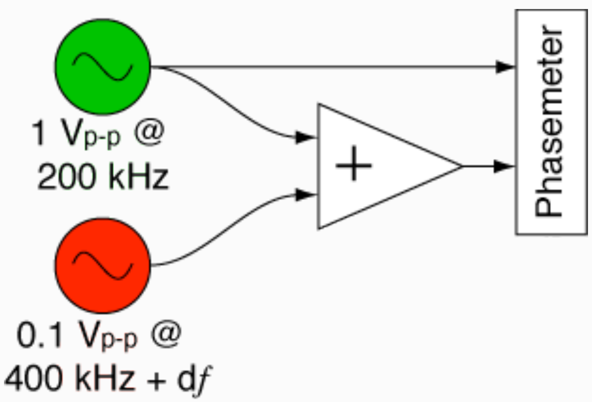
GSFC-JPL

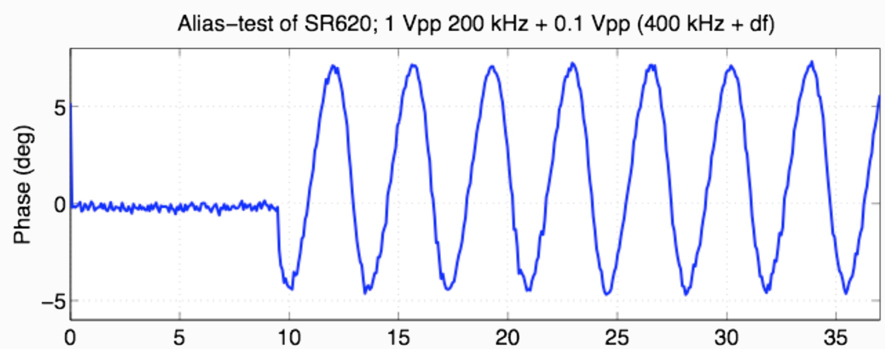
Phasemeter Requirements

- Science phasemeter must
  - Resolve the 1,000 cycles/√ Hz of laser noise to 3 μcycles/√ Hz @ 5 mHz (corresponding to 3 pm/√ Hz @ 5 mHz)
  - Track the frequency of the beat note, dominated by the annual variations in Doppler frequency (2 MHz to 20 MHz)
  - Multi-tone phase measurement and tracking capability for clock phase noise measurement
    - Secondary tones 1 MHz from carrier with -20 dBc amplitude.
  - Provide high speed output to lock slave laser to master laser with < 3 Hz/√ Hz relative noise (less than intrinsic laser noise).
    - Goal: Lock with < 2 µcycles/√ Hz to simplify TDI, reduce telemetry, etc.
    - Auto acquisition, auto gain, reconfigurable controller response (e.g phase-locking or arm-locking).

Why not zero-crossing phasemeter?

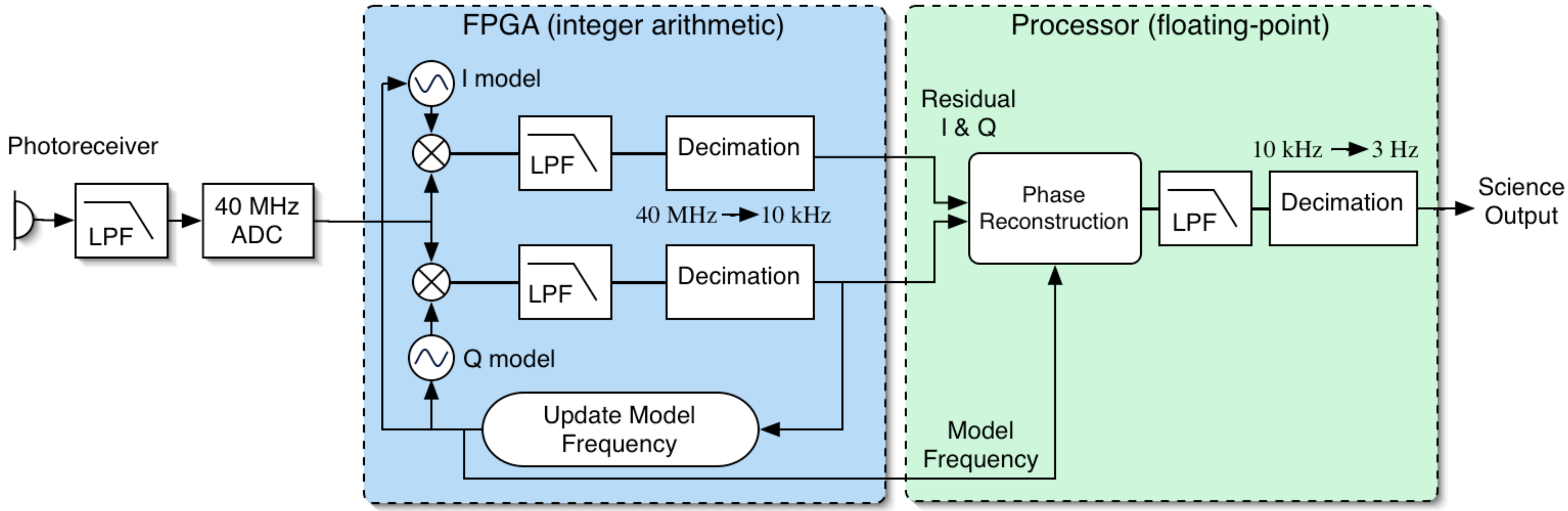
- No information between zero-crossing points.
  - Effective sampling rate = heterodyne frequency.
  - Introduces aliasing of noise from *2f, 3f, 4f,…* (and 0*f*)
- For LISA could have up to 10 harmonics.
  - Measurement noise increased √ 10 x shot noise ~ 30 pm/√ Hz.





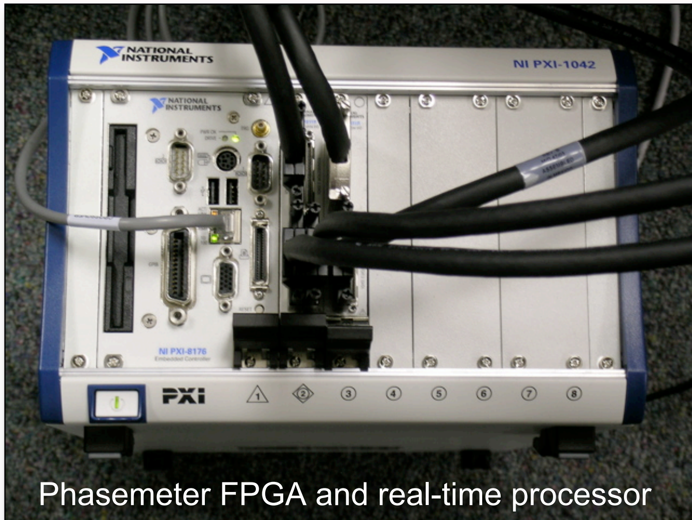
- Zero-crossing phasemeters are not well suited for LISA.
  - Broadband (shot) noise
  - Sub-shot noise phasemeter error allocation.

Science Phasemeter

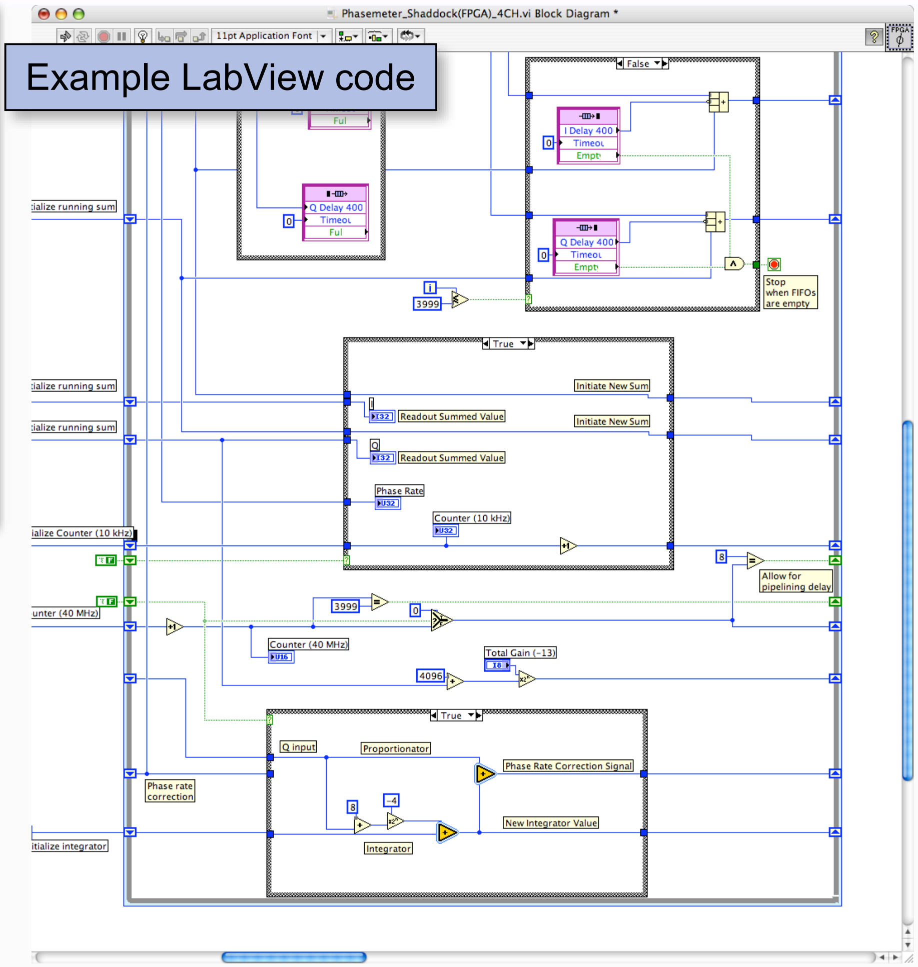


Target	Function	Input Samples/second	Output Samples/second
FPGA	Implement I-Q demodulation with digital phase locked loop	40 MHz	10 kHz
Processor	Reconstruct phase and decimate to 3 Hz	10 kHz	3 Hz

Breadboard Phasemeter



Phasemeter FPGA and real-time processor



Example LabView code

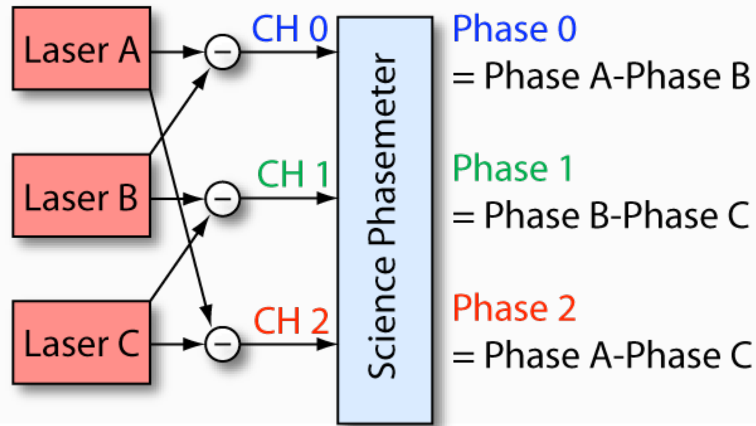
- FPGA programmed in LabView
  - uses off the shelf equipment.
  - 8 channels per FPGA.
  - One floating point processor handles all channels.
  - Science and Fast phasemeters share common ADCs.
  - Only linear phase filters used, avoids complicating data analysis.

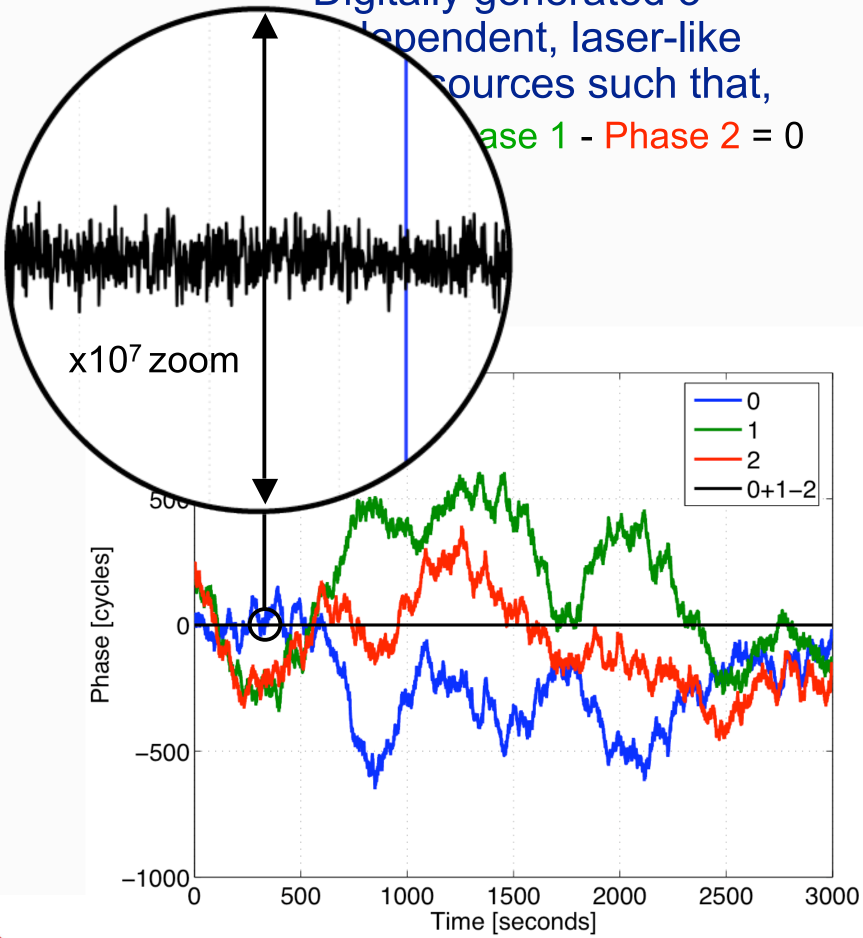
GSFC-JPL

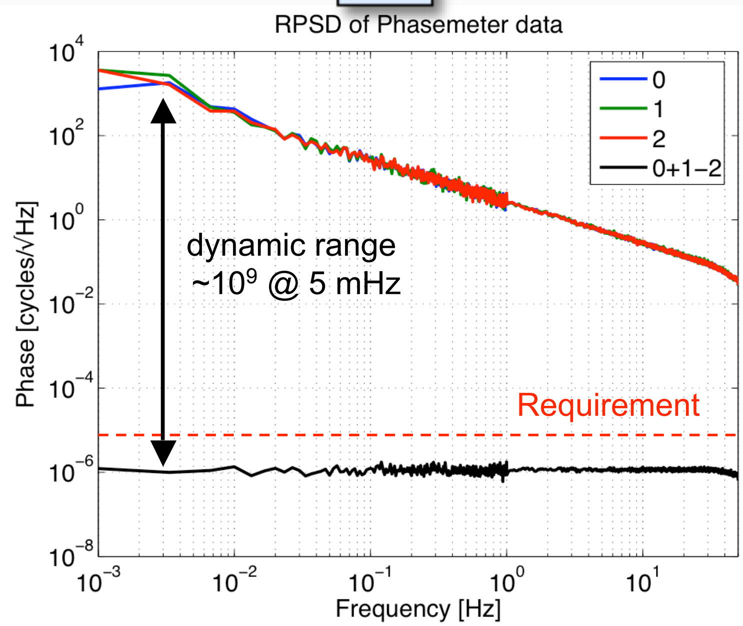
Science phasemeter testing

- Digitally tested dynamic range requirement.
  - Digitally generated 3 ependent, laser-like ources such that, ase 1 - Phase 2 = 0

Equivalent Optical Setup



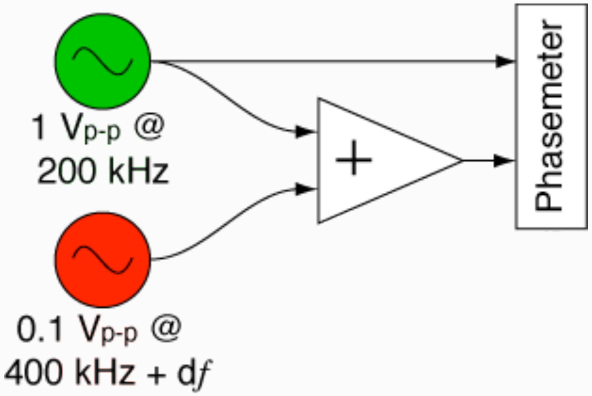


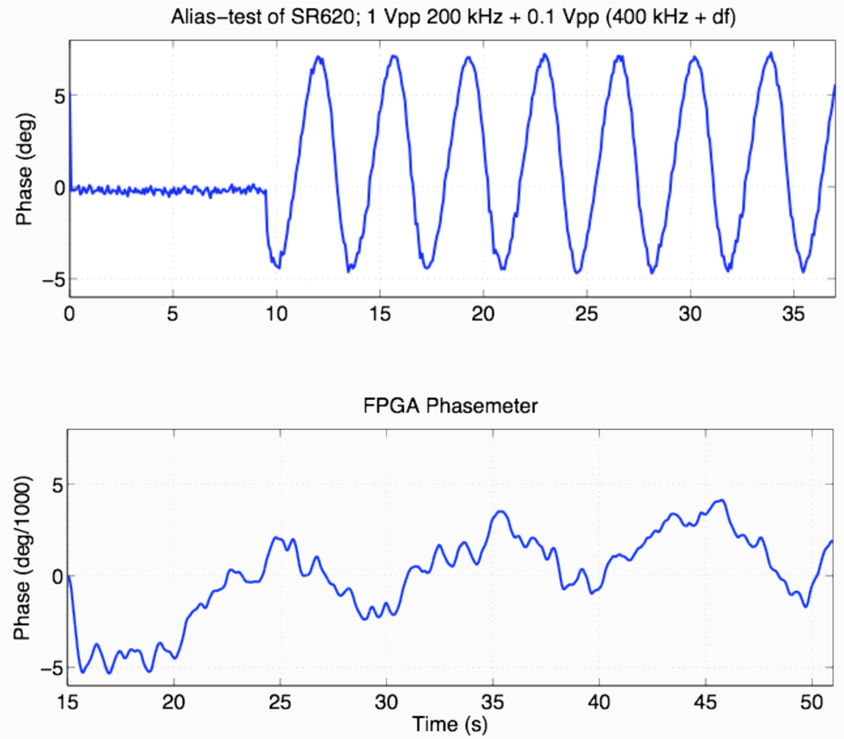


GSFC-JPL

Anti-aliasing

- Phasemeter designed to have aliasing suppression of 10^7 in the LISA signal band.





GSFC-JPL

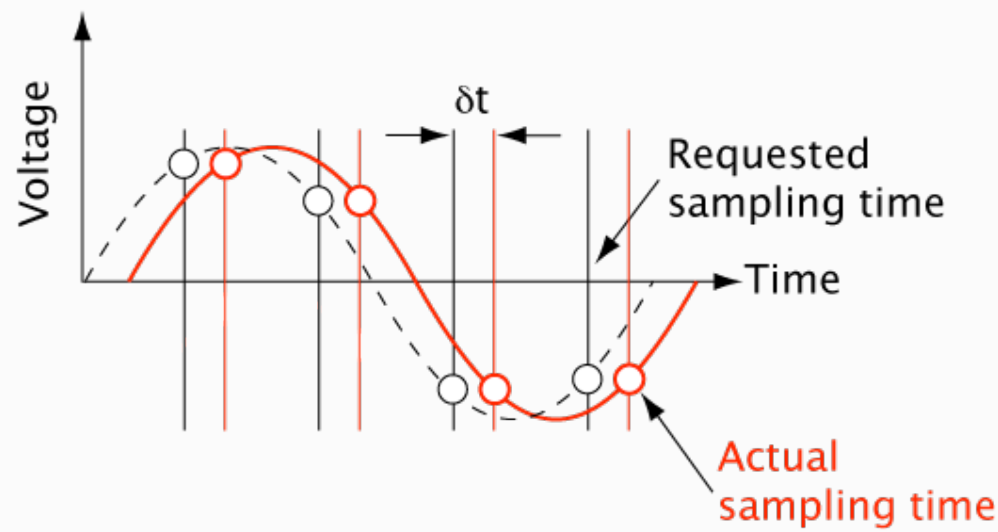
Sampling time jitter

- Jitter in the sampling time δt produces a phase error

$$\phi = \delta t \times f_{het}$$

- For 1 μcycle/√ Hz phase noise requirement, and a 20 MHz heterodyne frequency.

$$\delta t < 0.5 \times 10^{-13}\ \mathrm{s}/\sqrt{\mathrm{Hz}}$$

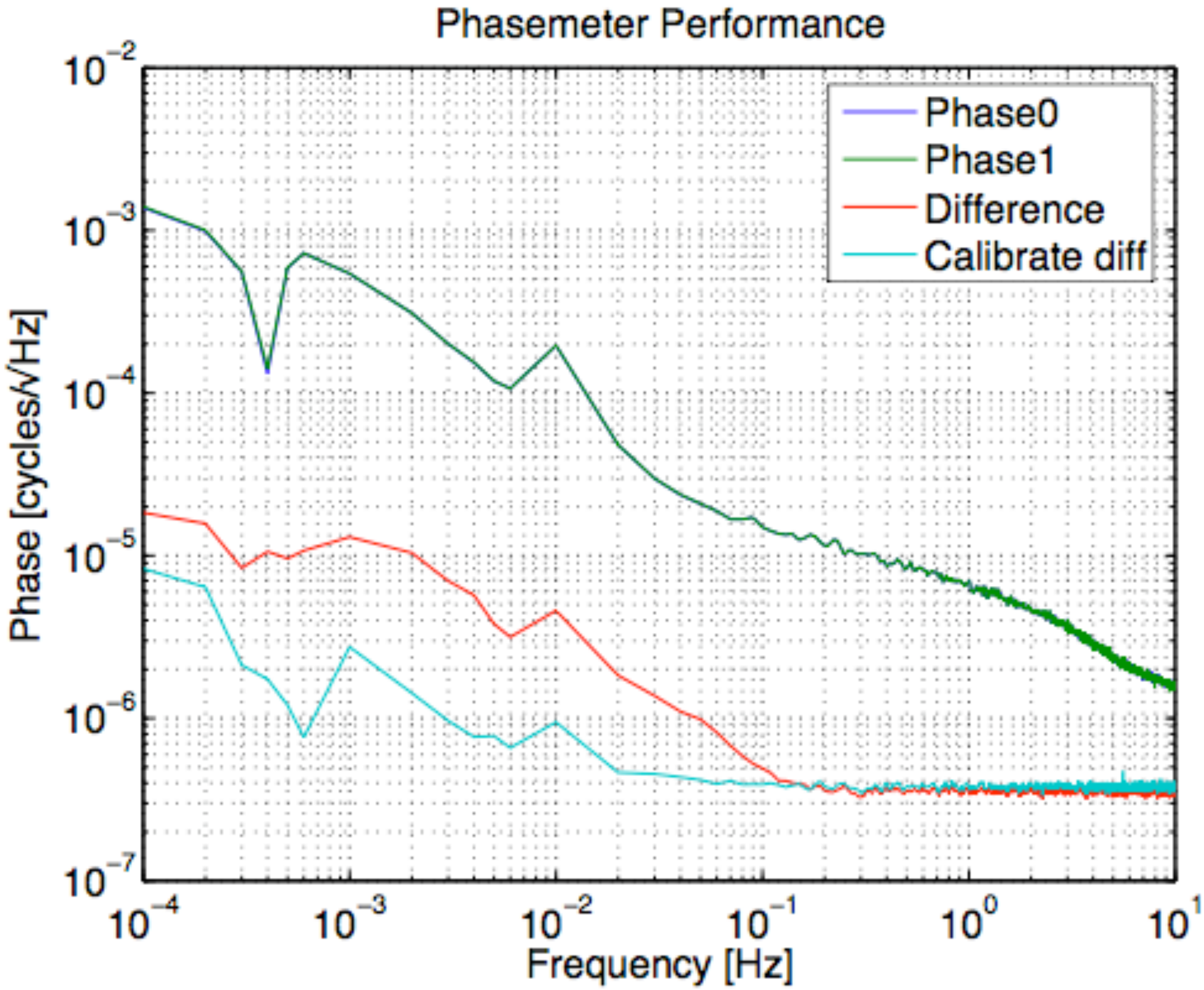


- Jitter in the sampling time arising from clock is already removed.
- Remaining sampling jitter is the fluctuating latency of the ADC.

Calibrate jitter by processing the phase of a known signal at a different frequency using the same ADC.

GSFC-JPL

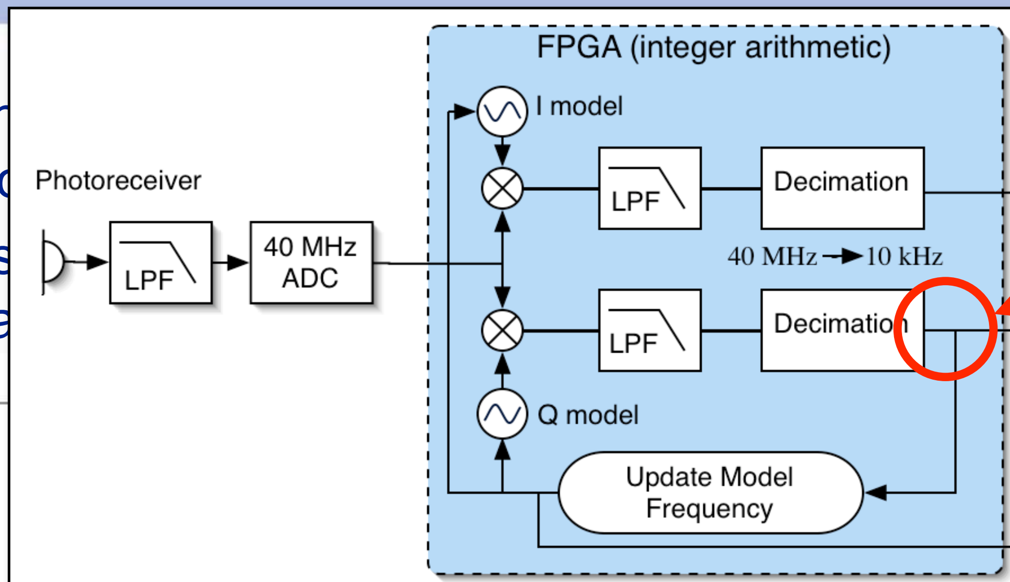
ADC jitter removal

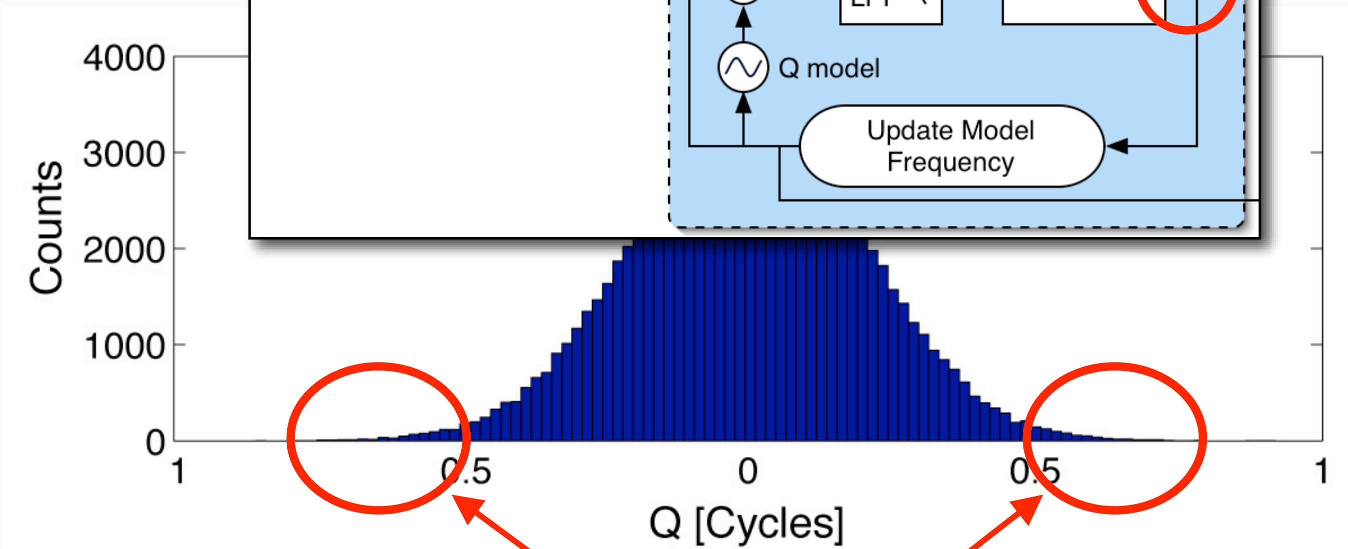


GSFC-JPL

Cycle Slipping

- The ph ... ed on the value c
- Values ... ed - feedba ... curs.





Cycle slipping occurs

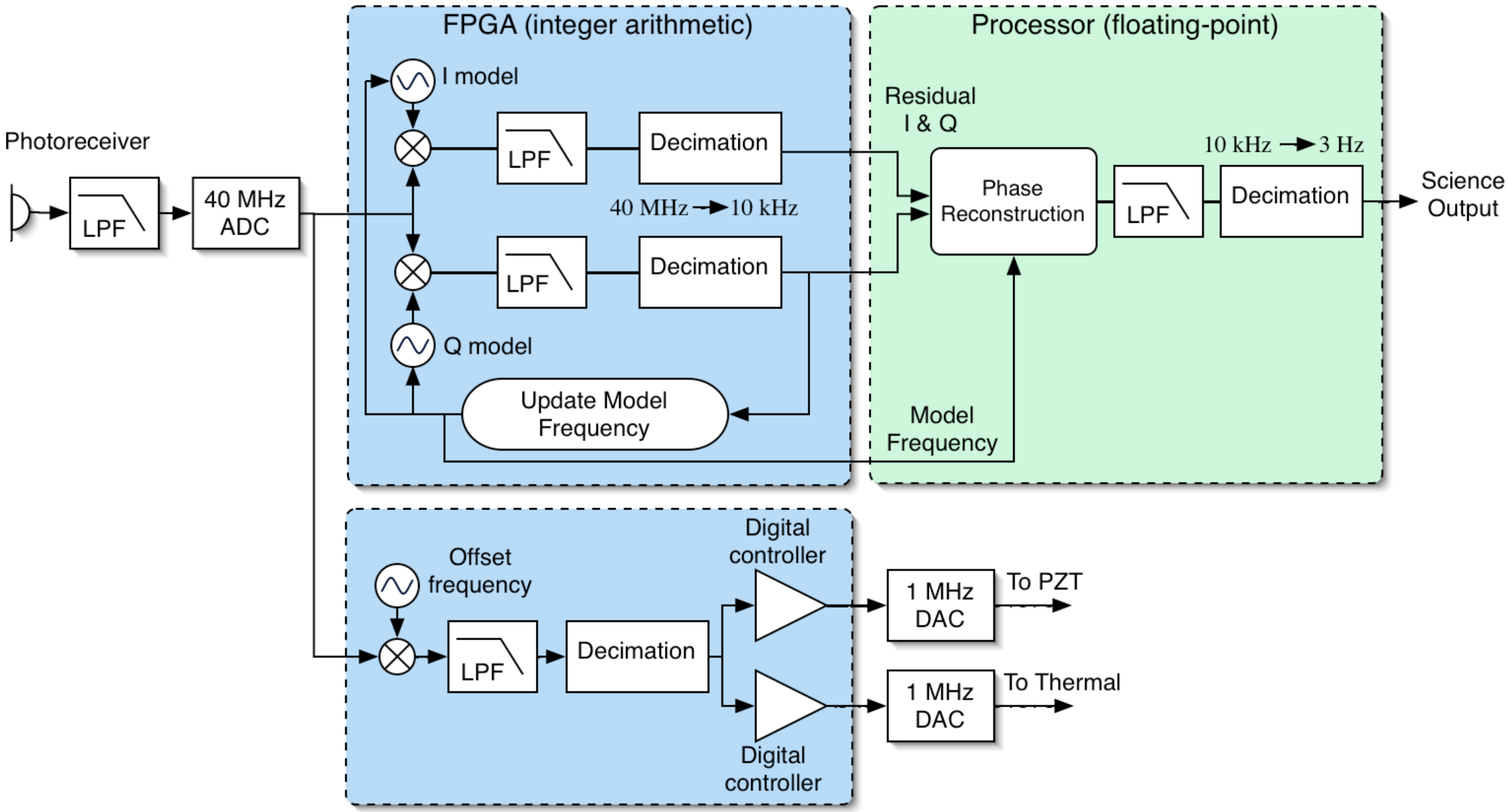
Cycle Slipping

- Cycle slipping is most sensitive to the input's high frequency noise.
  - Low frequency noise is suppressed by loop gain.
- 30 Hz/√ Hz white frequency noise is too high for current phasemeter.
  - Cycle slipping sets in around 12 Hz/√ Hz white noise.
- More realistic laser frequency noise rolls off.
  - 30 Hz/√ Hz with 1/f roll off above 400 Hz is okay.

Cycle Slipping Solutions:

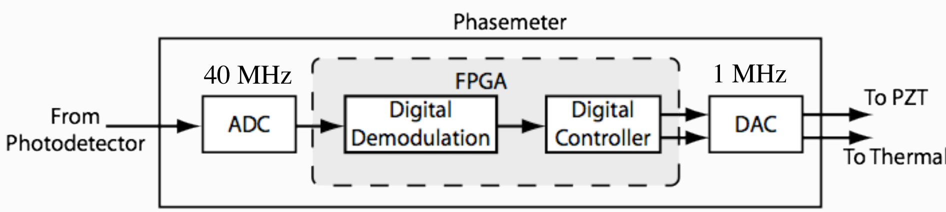
1. Tighten laser frequency noise requirement at high frequencies.
2. Increase digital phase-locked loop update rate to reduce the noise in Q.

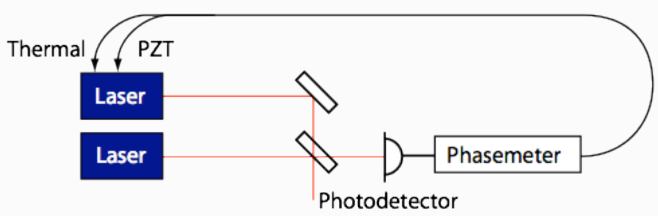
Laser Locking Output

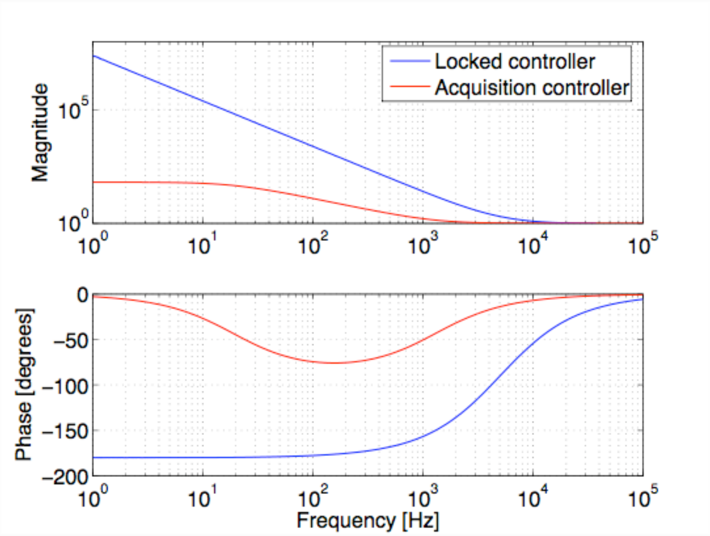


Laser Locking Output

- Low-latency phase measurement for laser phase-locking and arm-locking.
- All-digital controller implemented on reconfigurable FPGA.
- Uses same ADC as science phasemeter.
- Dynamically adjustable heterodyne frequency.
- Auto-acquisition mode driven by frequency counter (lasers need only be within 20 MHz).
- Automatically senses lock status and switches controller from a low-gain acquisition mode to the high-gain science mode.





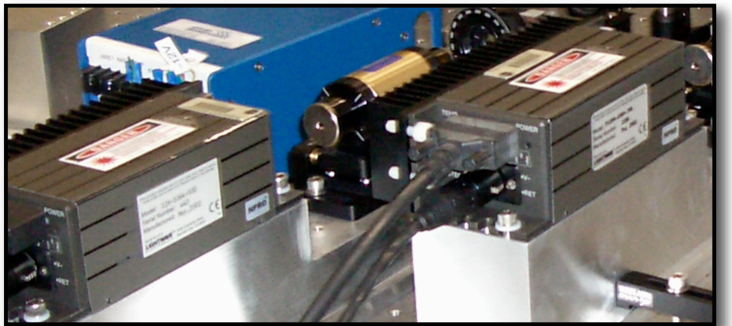


GSFC-JPL

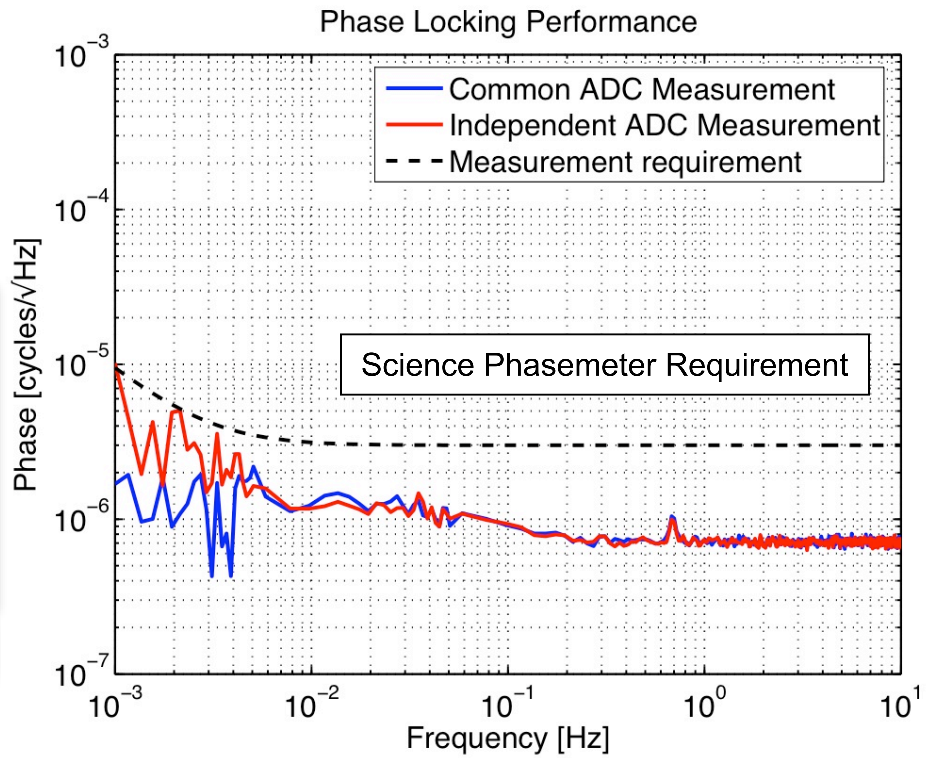
Laser Locking Output

The fast-phasemeter has been used to phase-lock two commercial NPRO lasers Maintains phase-lock indefinitely (weeks).

Used science phasemeter to evaluate locking performance.



Two lasers locked using fast phasemeter

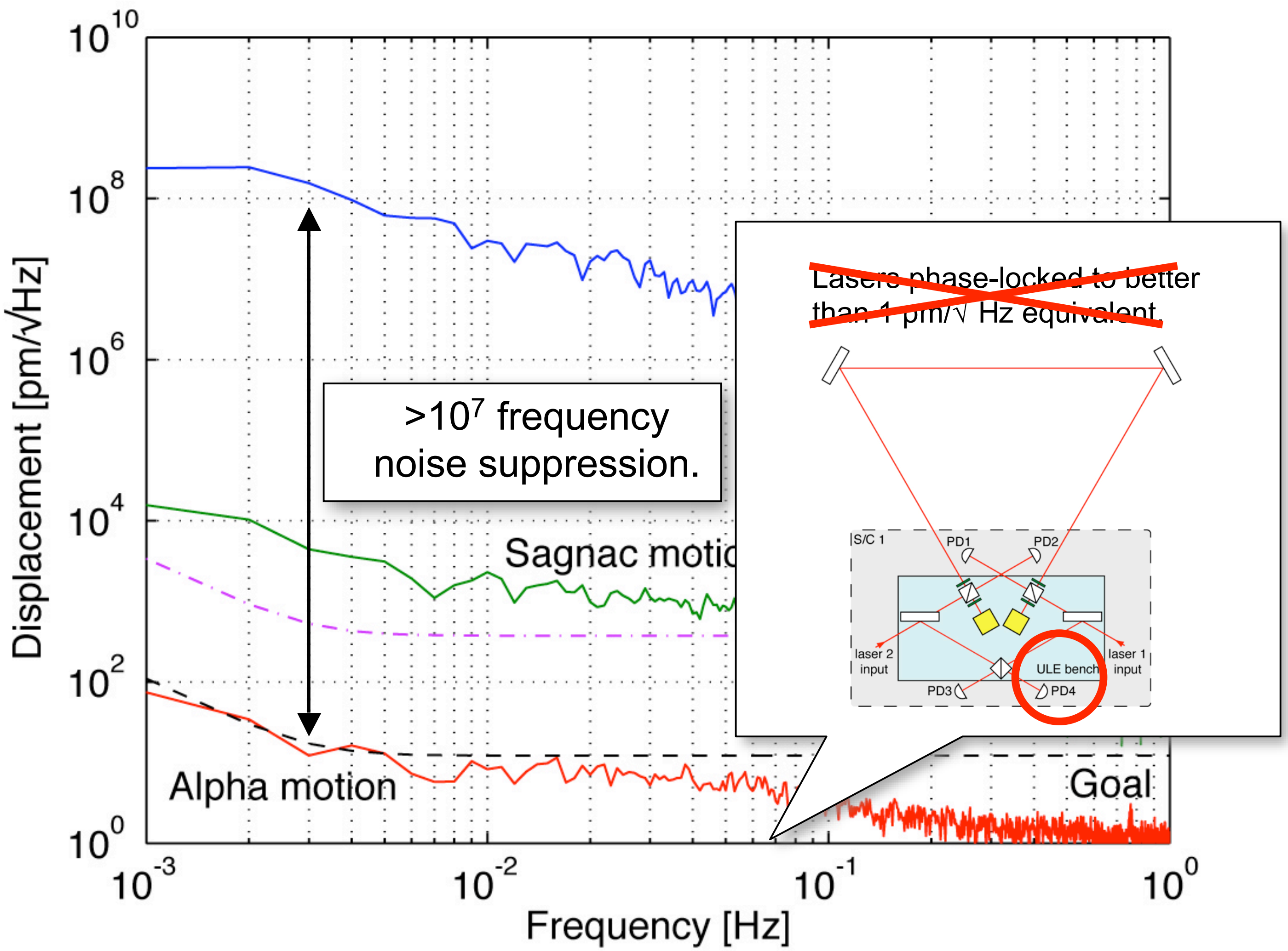


- Locked to < 1 μcycle/√ Hz above 100 mHz
- Locked to < 10 μcycle /√ Hz at 1 mHz
- Low frequency performance limited by ADC jitter.

Frequency Noise Cancellation

- Test phasemeter, photoreceivers, and frequency distribution system using representative signals.
  - 30 Hz/√ Hz frequency noise
  - 2-20 MHz heterodyne signal
  - 2-8 GHz sidebands for clock noise transfer
- System tests will characterize interactions between different errors.
  - Digital filter phase fluctuations (from independent clocks).
  - Frequency noise aliasing from multiple heterodyne frequencies.
  - Interpolation error in the presence of real-world phasemeter filtering and sampling jitter.
  - ADC harmonic distortion mixing with EOMs inter-modulation products.

Noise cancellation

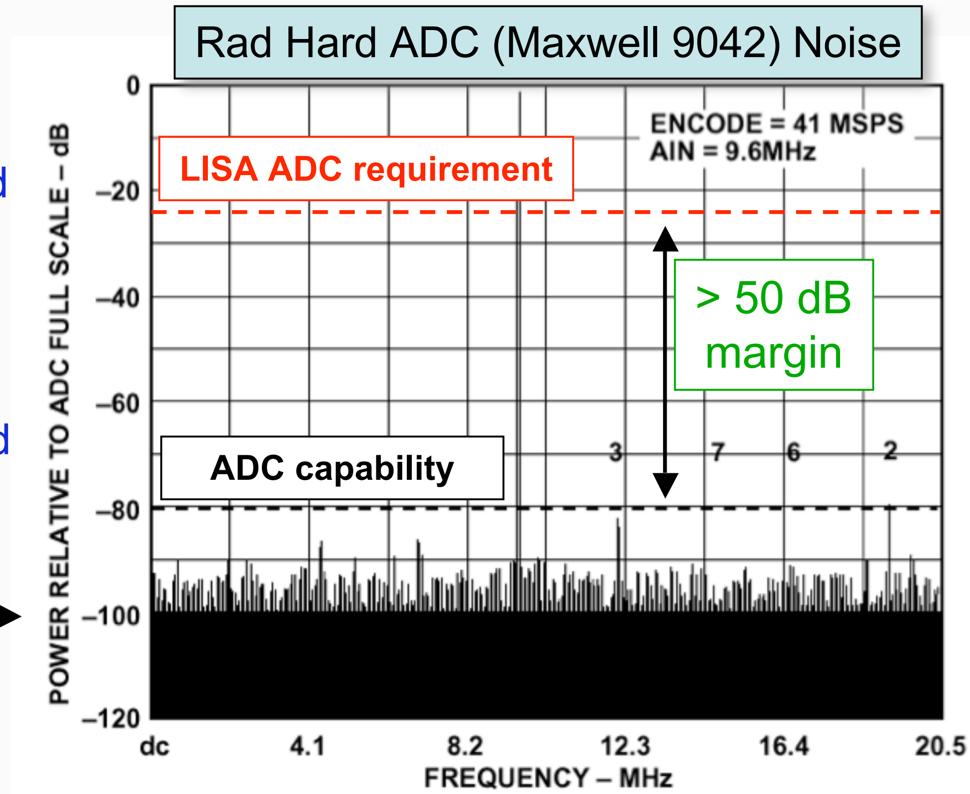


GSFC-JPL

Phasemeter technology readiness

- Phasemeter validated in laboratory
  - Analytical models of the phasemeter replicate the test data.

- Phasemeter path to flight
  - FPGA algorithms implemented with integer processing.
  - Floating-point processing requires only tens of kFlops.
  - Compatible radiation hardened ADCs identified e.g. Maxwell 9042:15 bit, 41 MS/s.



GSFC-JPL

Phasemeter Summary

- Breadboard phasemeter works very well.
  - Phasemeter has passed all digital and electronic tests.
  - Critical requirements have been demonstrated.
  - Optical/electronic tests of the phasemeter in a system environment are underway.
- Phasemeter has a clear path to flight. All components are off the shelf items.
  - Algorithms already developed - will perform identically on any FPGA/ASIC.
  - ADC requirements non-critical. Suitable rad-hard candidates available.

Future Work

- Increase sampling frequency to 80 MHz to ease analog filtering requirements.
- Improve DC phase accuracy via ADC calibration tones.
- Reduce susceptibility to cycle slipping